University of California, Berkeley Extension

Certificate Program in Semiconductor IC Design
Professional Sequence in Semiconductor Technology Fundamentals

EL ENG X484: Digital ICs
(2 semester units in EL ENG, Online Format)

Course Syllabus

A. Course Description

This state-of-the-art course begins with the solid understanding of digital operation principles and gradually channels into more complex entities, such as multiplexers and flash memory. Featuring in-depth illustration and broad discussions, this course distills essential concepts, SPICE verification, and design skills from CMOS, ECL, and BiCMOS logic, to memory design. This unique course provide you an opportunity working on a research project to address the compelling issues in cutting-edge technologies including embedded SRAM (eSRAM), non-volatile memory, and high-speed embedded DRAM.

B. Prerequisite

- *"X480: Introduction to Microelectronics"*
- *"X488: Semiconductor Devices for IC Design"*

or working-level knowledge on solid-state and digital electronics, such as

- *Inverter basics*
- *BJT & MOS I-V characteristics*
- *Channel-length modulation of MOSFET*
- *Body-effect of MOSFET*

C. Timeline

Timeline	Course events	Lecture pace
Day 30	**Homework 1**	30% of lectures done
Day 60	**Homework 2**	60% of lectures done
Day 90	**Homework 3**	100% of lectures done
Day 120	Final exam setup	
Day 120	**Midterm Exam**	
Day 150	Final exam date confirmed	
Day 150	Optional final project	Extra bonus
Day 165	**Proctored final exam**	
Day 180	Course end	Lecture ends

- Pacing yourself well is one of the key factors to succeed in this course. *Mark your calendar* for the timeline and course events. *Make a pla*n for studying lectures and then follow through.
- The course registration date (Day 1) is the date you receive the login information and welcome email.
- *You final exam request/setup process normally takes up to a couple of months to finalize. Therefore, it is strongly suggested you reserve the last two weeks (Day 165-180) for contingency.*
- *The official course end date is Day 180*, which is different from what you see on the classroom site where we add 20 additional days for pre-compensating technical access issues.

D. Required Readings

PDF Slides (Downloadable in the Classroom).

E. Learning Objectives

Upon successful completion of the course, students will be able to

- Perform the digital circuit static and dynamic analysis to the transistor level.
- Get a comprehensive understanding of the digital IC design with topics covered CMOS , ECL, BiCMOS, and memory design.
- Possess the intuitive skill to forecast the analysis results.
- Use SPICE to verify hand-analysis results and illustrate complex behavior outside the scope of manual analysis.
- Independently work on a research project with topics covered eDRAM, eSRAM, and non-volatile memory.

F. Intended Audience

This course is intended for technical professionals who want to enter the semiconductor market and are looking to acquire advance knowledge in this area.

G. Course Content Outline

Session 1. Digital Circuits Basics

Basic digital circuit concepts and definitions of important parameters such as logic levels, noise margins, and propagation delay will be reviewed. The students will learn how to conduct a thorough analysis for static and dynamic characteristics of a digital inverter—the nucleus of all digital circuit designs.

- *Static Behavior of Digital Inverters*
- *Dynamic Behavior of Digital Inverters*
- *Key Concepts of Logic Circuit Design*

Session 2. Static CMOS Digital Circuits

The students will learn the graphical skills to tackle the complementary devices in one circuit and use a methodology to derive the transfer characteristics, dynamic power dissipation and power dissipation of CMOS Inverters. Rather than go through the tedious integration calculation, the instructor will use a simple method

combined with the important graphical concept, totally understand its dynamic behavior, and estimate the propagation delay.

- *Evaluating Robustness of CMOS Inverter*
- *Evaluating Power Consumption of CMOS Inverter*
- *Evaluating Speed Limitation of CMOS Inverter*
- *Design of Static CMOS Logic Circuits*

Session 3. Advanced CMOS Digital Circuits

This session will stress on not only the fundamental static and dynamic characteristics with respect to each style but how to choose a logic style from a design perspective. Topics covered include pseudo-NMOS logic, PTL logic, dynamic CMOS, and domino logic.

- *Evaluating Robustness & Speed of Pseudo-NMOS Inverter*
- *Evaluating Speed Limitation of CMOS Pass-Transistor Logic*
- *Noise Consideration of Dynamic CMOS Logic Design*
- *Timing Issues Dynamic CMOS & Domino Logic*

Session 4. Semiconductor Memory Design

Memory is an inarguably imperative subject because not only a large portion of silicon chip in modern digital circuits is used for storing complex program instructions and tremendous amount of data but also the majority of MOSFETs are dedicated to cache memories in today's state-of-the-art microprocessor. Topics include static sequential circuits static random-access memory (SRAM), dynamic random-access memory (DRAM) and peripheral circuitry such as single-ended sense amplifier and differential-mode sense amplifier with dummy cell, read-only memory (ROM), including erasable programmable read-only memory (EPROM) and flash memory. For the last one, recently NOR flash architectures continue to tackle the requirements of faster XIP (eXecute In Place) in the wireless communications. Device structure, hot-electron injection phenomenon, programming principle, and applications will be presented.

- *Static Sequential Circuits: Key Concepts*
- *Static Random-Access Memory (SRAM)*
- *Dynamic Random-Access Memory (DRAM)*
- *Memory Peripheral Circuitry: Sense Amplifier Design*
- *Nonvolatile Read-Only Memory*

Session 5. High-Performance Digital Circuits

Considering a comparable technology, the speed of ECL gate is about two to five times faster than that of its CMOS counterpart. ECL design considerations including reference voltage, logic levels, and noise immunity will be discussed. On the other hand, combining the low-power consumption, high noise immunity and high-density integration of MOS digital circuits with the high current-driving capability of BJT ones, BiCMOS logic has opened a new opportunity to achieve higher performance. Some of the design schemes such as the voltage swing and propagation delay will be addressed.

- *Bipolar Emitter-Coupled Logic Gate*
- *Evaluating Robustness and Noise Immunity of ECL Gate*

- *Designing BiCMOS Digital Circuits*

H. Course Length

- The 30-hour course length covers not only the audio runtime but also the time to catch up by rewinding and replaying video. It also includes the time to take notes and to communicate/discuss with the instructor.
- Other than the 30-hour course length, you are expected to spend additional 60 hours studying the lectures, digesting the materials, working on the assignments, and preparing for the exams.
- Most students watch the lecture video or read PDF slides two or three times before they can fully grasp the concepts, cultivate problem-solving skills, and have a good grade on the final exam.

I. Course Grade Weighting (Grading)

The student's cumulative grade in the course will be based on the following criteria:

- Discussion Participation: 10 points
- Progress Updates: 10 points
- Written Homework Assignments: 30 points
- Midterm Exam (Take-home exam): 20 points
- Final Exam: 30 points
- Optional Final Project (Extra bonus up to 10 points): 0 to 10 points

You must pass the final exam with a grade of at least 70 percent to pass the course.